AVINASH KUMAR MISHRA

Power Electronics Engineer | VLSI & FPGA Design | Embedded Systems | 4-Layer PCB Design
+91-7372986669 | kumarmishra.793@gmail.com | linkedin.com/in/avinash-mishra-172b18165

PROFESSIONAL SUMMARY

Electronics engineer focused on power electronics and hardware design, specializing in resonant/switch-mode converters, magnetics, and 4-layer PCB layout, backed by circuit-level simulation in MATLAB and SPICE. Hardware Intern at OLA Electric, working on 1kW EV charger schematics/PCB layout in Altium and CAN-based EOL validation for BESS inverters. Independently designed and debugged a 4-layer CAN FD transceiver PCB end-to-end. Also proficient in FPGA/RTL design (Verilog, SystemVerilog) from a signal processing background.

EDUCATION

Master of Technology — Signal Processing and Machine Learning | CGPA: 8 **2024 – 2026**
National Institute of Technology Karnataka (NITK), Surathkal, Karnataka

Bachelor of Technology — Electronics and Communication Engineering | CGPA: 7.73 **2018 – 2022**
Punjabi University, Patiala, Punjab

INTERNSHIP EXPERIENCE

Hardware Intern **2026 – Present**
OLA Electric, Bengaluru, Karnataka

- Engineered an End-of-Line (EOL) validation system for 4–9 kW BESS inverters using CAN bus protocol, automating functional testing on the production line, reducing manual inspection time by 40% and improving fault detection accuracy by 25%.
- Built the EOL test setup end-to-end, including test fixture and hardware bring-up, integration of test equipment, and automation scripts, streamlining validation across the production line and cutting test cycle time by 30%.
- Designed schematic diagrams and PCB layouts for EV chargers in Altium Designer, handling component selection, power stage layout planning, and design reviews to meet electrical safety.
- Performed testing and validation of 1kW EV chargers, verifying functional performance and compliance with design specifications before production release.

PROJECTS

1kW LLC Resonant DC-DC Converter Design (400V-60V) for Battery Charging Applications

- Designed a full-bridge LLC resonant converter (400V-60V, 16A) targeting a calculated 98.95% efficiency, with component selection from real datasheets — SiC primary MOSFETs (Wolfspeed) and synchronous rectification (Infineon OptiMOS) in place of diode rectification, cutting rectifier loss by ~85%.
- Cross-validated the resonant tank, magnetics (Ferroxcube ETD cores), and full loss budget (10.16W on 960W output) across MATLAB and two independent SPICE engines (ngspice, LTspice), catching a real voltage-margin issue from integer-turns rounding invisible in the idealized hand calculation.

4-Layer CAN FD Transceiver PCB Design

- Designed a 4-layer CAN FD interface board from schematic to layout, integrating an SPI-based CAN controller and CAN transceiver stage with ESD-protected, terminated CAN bus (TVS array + jumper-selectable 120Ω termination) and a two-stage 24V-5V-3.3V power path to correctly level-match logic across the controller, transceiver, and host MCU.
- Diagnosed and resolved multi-layer routing, ground-plane continuity, and via-connectivity issues during layout; verified full schematic and PCB connectivity through systematic net-level checks before finalizing the design.

Wireless Endoscopic Capsule (M.Tech Major Project)

- Engineered an FPGA-based image processing pipeline and System-on-Chip (SoC) architecture for a wireless endoscopic capsule using Verilog HDL on the Zynq-7000 platform.
- Applied color transformation and block compressive sensing algorithms, reducing data bandwidth by 60% while preserving image quality.

Asynchronous FIFO - Design and Verification (SystemVerilog)

- Architected a parameterized dual-clock FIFO featuring Gray code pointer synchronization and dual flip-flop synchronizer to eliminate metastability across clock domains.
- Developed and verified using a SystemVerilog testbench with SVA assertions and constrained-random stimulus, achieving 98% functional coverage.

Single-Cycle RV32I RISC-V Processor (Verilog)

- Architected a complete single-cycle RISC-V processor in Verilog, covering the ALU, register file, instruction memory, fetch unit, and control unit to support the full RV32I ISA.
- Achieved single-cycle execution for every instruction, delivering a straightforward and predictable hardware pipeline verified through simulation testbenches.

TECHNICAL SKILLS

Languages: Verilog, SystemVerilog, C, Python (scripting/automation)

Tools: Vivado, Quartus Prime, ModelSim, EDA Playground, Cadence, Altium, KiCad, Logisim, CANalyzer, Vector CANoe

Core Skills: FPGA Programming & Testing, ASIC Design, RTL Design & Verification, VLSI Physical Design, IC Design, System-on-Chip (SoC) Design, Embedded Systems, Hardware Description Language (HDL), PCB Design & Multilayer Layout, Testbench Development, Debugging, Digital Signal Processing, Image Processing & Computer Vision, Digital Electronics, Power Electronics, Low-Power VLSI

Foundational Knowledge: ADC/DAC Interfacing, Static Timing Analysis (STA), Analog Electronics

Soft Skills: Problem Solving, Teamwork, Communication, Critical Thinking, Time Management, Attention to Detail

Areas of Interest: Logic Synthesis, High-Performance Computer Architecture (HPCA), Digital IC Design, Circuit Analysis