AYUSHI JAIN

Seeking an experience driven role as an ASIC Digital Design and Verification Engineer, leveraging 1 year of hands-on expertise in Digital Electronics, Verilog, SystemVerilog and verification methodologies to contribute to PHY level verification.

9643088999 jayushi2703@gmail.com Linkedin

CORE COMPETENCY

• Digital Electronics	• VMM	• Agile Methodologies
• Verilog	• UVM Methodologies	• Performance Optimization
• SystemVerilog	• Debugging & Troubleshooting	• Static Timing Analysis

TECHNICAL SKILLS

Hardware Description Languages: Verilog, System Verilog.
Protocol and Standards: HDMI 2.1, ATE (Automated Test Equipment).
EDA Tools: Verdi, DVE.
Test and Debug: ATE debug flow, Regression setup, Waveform analysis.
Version Control and Collaboration: Perforce, JIRA, Confluence.

SOFT SKILLS

- Communicator
- Team Player
- Analytical
- Attention to Detail
- Collaborator

WORK EXPERIENCE

Synopsys, Noida **Sept 2024 -Present**
ASIC Digital Design Intern
Projects:

HDMI 2.1 RX

- HDMI is a high-speed digital interface used for transmitting video and audio data. It handles adaptive equalization, clock recovery, and protocol compliance to ensure accurate signal decoding.
- Developed functional checkers for HDMI RX block to monitor and validate calibration and adaptation sequences and integrate it into VMM testbench.
- Collaborated with design team to refine specs and ensure functional correctness across all HDMI modes.
- Performed debugging and waveform analysis using tool like Verdi and DVE.

AUTOMATED TEST EQUIPMENT

- ATE (Automatic Test Equipment) simulation environments are used during the pre-silicon phase to validate test patterns and ensure they behave correctly before silicon fabrication.
- Developed and maintained ATE Testbench setup for running automated testcases.
- Executed regression run across multiple suites and product configuration.

TRAINING

Industrial training SEE Training by Mentor Graphics conducted by 3ST Technologies Pvt. Ltd. Jan 2024 to Aug 2024
Training encompassed a comprehensive understanding of Verilog, Digital Electronics, STA, CDC, and SystemVerilog. Also involved in practical projects to apply and reinforce these skills.
Projects:

UART Communication Protocol using Verilog

- UART (Universal Asynchronous Receiver/Transmitter) is a serial communication protocol that transmits 8-bit data frames.
- It including special bits like start, stop, and optional parity bits, using an agreed-upon baud rate for asynchronous communication.

I2C Protocol using Verilog

- I2C (Inter-Integrated Circuit) is a serial communication protocol where a single master initiates communication and controls the clock signal.
- The master's requests is responded by single slave over two bidirectional lines, SDA and SCL.

COLLEGE PROJECTS

Projects:

House Rent Price Prediction using Machine Learning

- Built a predictive model using regression techniques to estimate house rent prices based on features like location, size, and amenities.
- Demonstrated ability to apply machine learning concepts for solving real-world problems.

Obstacle Avoiding and Fire Fighting Robot

- Designed and implemented an autonomous robot using sensors for obstacle detection and fire source identification.
- Integrated motor control and flame detection modules to ensure real-time obstacle avoidance and fire extinguishing functionality.

Sense Amplifier (VLSI Project)

- Designed and simulated a sense amplifier circuit for reliable read operations in SRAM.
- Gained hands-on experience in CMOS circuit design and simulation using EDA tools

EDUCATION

- B.Tech. (Electronics and Communication Engineering) from Bharati Vidyapeeth College of Engineering, Delhi 2024 securing 9.14 CGPA and rank 3rd in college.
- 12th from Queen Mary's School, Delhi in 2019 securing 94.5% in CBSE Boards.

PERSONAL DETAILS

Date of Birth: 27th Mar 2001 **Address:** Delhi
Languages Known: English, Hindi