HARSHAL PATIL

+91 8605100583 • harshalspatil21@gmail.com • LinkedIn • GitHub • Pune, Maharashtra

PROFESSIONAL SUMMARY

Embedded Firmware Engineer with 3 years of experience in optimizing and validating safety-critical firmware for automotive Battery Management Systems (BMS) on ARM Cortex-M platforms. Proven track record in optimizing peripheral drivers (SPI, I2C, UART) to achieve a 30% increase in communication throughput and a 25% reduction in power consumption. Expert in MISRA-C compliance, RTOS (FreeRTOS), and automated testing using Python and CAPL. Seeking leverage expertise in real-time systems and hardware-software integration for Consumer Electronics R&D roles.

TECHNICAL SKILLS

Languages: C (Embedded), C++ (OOP), Python, CAPL, Assembly

RTOS: FreeRTOS, Bare metal

Microcontrollers: STM32 (Cortex-M4), ARM Cortex-M Series, 16/32-bit MCUs

Protocols: CAN (SAE J1939), SPI, I2C, UART

Tools: Git/GitHub, CANoe, Eclipse IDE, GHS Debugger, Imagix (Static Analysis), Logic Analyzer

Standards & Methodologies: MISRA-C, ISO 26262 (Functional Safety), Agile/Scrum, Code Review, Unit & System Level Testing

PROFESSIONAL EXPERIENCE

Automotive Embedded Systems Engineer, Tata Consultancy Services *Oct 2023 – Present*

Client Project(Japanese Automotive client): Battery Management System (BMS) Firmware — Automotive Domain

- **Firmware Development & Optimization:** Optimized SPI, UART, and I2C peripheral drivers in Embedded C for a high-voltage BMS, achieving a 30% improvement in bus communication speed and a 25% reduction in active power consumption.
- **Driver Development & Integration:** Boosted data throughput by 35% through the optimization of low-level CAN and SPI drivers for real-time telemetry.
- **Code Quality & Standards Compliance:** Led code review sessions and enforced MISRA-C and ISO 26262 standards across the team, improving firmware reliability by 40%.
- **Test Automation:** Authored Python test scripts and CAPL sequences in CANoe to automate 80% of unit and system-level regression tests, reducing manual testing effort and accelerating sprint validation cycles.
- **System Testing & Debugging:** Drove system-level debugging using Imagix and CANoe, achieving a 98% defect detection rate and reducing average debugging cycle time by 30% across quarterly validation phases.

PROJECTS

STM32 Real-Time Clock (RTC) System *Oct 2025 – Nov 2025*

Technologies: STM32F407 (ARM Cortex-M4) · DS1307 RTC · I2C (HAL) · SysTick Timer · C

- Designed a precise timekeeping system with STM32F407 as I2C Master and DS1307 as Slave, implementing full HAL-based register read/write for time and date synchronization.
- Leveraged SysTick Timer to trigger periodic 1 ms/1 s interrupts, reducing CPU polling overhead and optimizing power efficiency through interrupt-driven scheduling.
- Validated I2C signal integrity using a logic analyzer, confirming protocol compliance and stable data transfer at 400 kHz Fast Mode.

EDUCATION

B.E. in Electronics & Telecommunication Engineering, Wadia College of Engineering *March 2019 - April 2023*

Specialization: Honours in Internet of Things (IoT) *CGPA: [8.39]*